IN THE CLAIMS

1. (original) A system, comprising:

a controller; and

a memory device coupled to the controller to receive signals therefrom, and comprising:

an array of memory cells arranged in a plurality of addressable banks, each bank comprises addressable rows and columns of memory cells;

a mode register; and

address circuitry coupled to the mode register to configure the addressable banks in response to a program state of the mode register.

2. (original) The system of claim 1 wherein the addressable banks can be configured as either four or eight banks.

3. (original) The system of claim 1 wherein the address circuitry selectively routes address signal to either a row decoder or a bank decoder in response to the mode register.

4. (original) A system, comprising:

a controller; and

a dynamic random access memory device coupled to the controller and comprising:

an array of X memory cells;

a mode register; and

address circuitry coupled to the mode register to configure the array in response to a program state of the mode register, wherein the mode register defines a number of addressable banks of the array.

5. (original) The system of claim 4 wherein a first state of the mode register configures the array into Y banks each having X/Y memory cells, and a second state of the mode register configures the array into Z banks each having X/Z memory cells.

6. (original) The system of claim 4 wherein the address circuitry comprises column, row and bank address decoders.

7. (original) The system of claim 6 wherein the address circuitry routes a selected address input signal to either the row or bank decoder in response to the mode register.

8. (original) The system of claim 7 wherein the address circuitry comprises a multiplex circuit.

9. (original) A system, comprising:

a controller; and

a synchronous dynamic random access memory (SDRAM) coupled to the controller and comprising:

an array of X memory cells;

a mode register;

a column address decoder;

a row address decoder;

a bank address decoder; and

address signal circuitry coupled to a plurality of address signal input connections, the address signal circuitry routes a selected one of the plurality of address input connections to either the row or bank address decoder in response to data stored in the mode register.

10. (original) The system of claim 9 wherein a first state of the mode register configures the array into Y banks each having X/Y memory cells, and a second state of the mode register configures the array into Z banks each having X/Z memory cells.

11. (original) The system of claim 10 wherein X = 4 and Z = 8.

12. (original) A system, comprising:

a controller; and

a synchronous dynamic random access memory (SDRAM) coupled to the controller and comprising:

an array of X memory cells;

at least one external input connection to receive a configuration signal;

logic circuitry coupled to the at least one external input connection;

a column address decoder;

a row address decoder;

a bank address decoder; and

address signal circuitry coupled to a plurality of address signal input connections, the address signal circuitry routes a selected one of the plurality of address input connections to either the row or bank address decoder in response to the logic circuitry.

13. (original) The system of claim 12 wherein a first state of the logic circuitry configures the array into Y banks each having X/Y memory cells, and a second state of the logic circuitry configures the array into Z banks each having X/Z memory cells.

14. (original) The system of claim 13 wherein X = 4 and Z = 8.

15. (original) The system of claim 12 wherein the at least one external input connection comprises two input connections to receive a two-bit configuration signal.

16. (original) A system, comprising:

a controller; and

a memory device coupled to the controller to receive signals including an input signal therefrom, and comprising:

an array of memory cells arranged in a plurality of addressable banks, each bank comprises addressable rows and columns of memory cells;

a decode circuit to decode the input signal; and

address circuitry coupled to the decode circuit to configure the addressable banks in response to a program state of the input signal.

17. (original) The system of claim 16 wherein the addressable banks can be configured as either four or eight banks.

18. (original) The system of claim 16 wherein the address circuitry selectively routes address signal to either a row decoder or a bank decoder in response to the input signal.

19. (original) The system of claim 16, wherein the input signal is a one-bit binary input.

20. (original) The system of claim 16, wherein the input signal is a multi-bit binary input and the number of banks is configurable.

21. (original) The system of claim 20, wherein the number of banks is four or eight.

22. (original) A system, comprising:

a controller providing an input signal; and

a dynamic random access memory device coupled to the controller and comprising:

an array of X memory cells;

a decode circuit to decode the input signal; and

address circuitry coupled to the decode circuit to configure the array in response to a program state of the input signal, wherein the input signal defines a number of addressable banks of the array.

23. (original) The system of claim 21 wherein a first state of the input signal configures the array into Y banks each having X/Y memory cells, and a second state of the input signal configures the array into Z banks each having X/Z memory cells.

24. (original) The system of claim 22 wherein the address circuitry comprises column, row and bank address decoders.

25. (original) The system of claim 24 wherein the address circuitry routes a selected address input signal to either the row or bank decoder in response to the controller input signal.

26. (original) The system of claim 22 wherein the address circuitry comprises a multiplex circuit.

27. (original) A memory device, comprising:

an array of memory cells arranged in a plurality of addressable banks, each bank comprises addressable rows and columns of memory cells;

a decode circuit to decode an external input signal; and

address circuitry coupled to the decode circuit to configure the addressable banks in response to a program state of the external input signal.

28. (original) The memory device of claim 27 wherein the addressable banks can be configured as either four or eight banks.

29. (original) The memory device of claim 27 wherein the address circuitry selectively routes address signal to either a row decoder or a bank decoder in response to the external input signal.

30. (previously presented) A dynamic random access memory comprising:

an array of X memory cells;

a decode circuit to decode an external input signal; and

address circuitry coupled to the decode circuit to configure the array in response to a program state of the external input signal, wherein the input signal defines a number of addressable banks of the array.

31. (previously presented) The dynamic random access memory of claim 30 wherein a first state of the input signal configures the array into Y banks each having X/Y memory cells, and a second state of the mode register configures the array into Z banks each having X/Z memory cells.

32. (original) The dynamic random access memory of claim 30 wherein the address circuitry comprises column, row and bank address decoders.

33. (original) The dynamic random access memory of claim 32 wherein the address circuitry routes a selected address input signal to either the row or bank decoder in response to the external input signal.

34. (original) The dynamic random access memory of claim 33 wherein the address circuitry comprises a multiplex circuit.

35. (original) A synchronous dynamic random access memory (SDRAM) comprising:

an array of X memory cells;

a decode circuit to decode an external input signal;

a column address decoder;

a row address decoder;

a bank address decoder; and

address signal circuitry coupled to a plurality of address signal input connections, the address signal circuitry routes a selected one of the plurality of address input connections to either the row or bank address decoder in response to data decoded by the decode circuit.

36. (original) The SDRAM of claim 35 wherein a first state of the external input signal configures the array into Y banks each having X/Y memory cells, and a second state of the external input signal configures the array into Z banks each having X/Z memory cells.

37. (original) The SDRAM of claim 36 wherein X = 4 and Z = 8.

38. (original) A method of operating a memory device comprising:

receiving an external input signal at decode circuitry of the memory device; and

adjusting address circuitry of the memory device in response to the decoded external input signal, wherein the address circuitry configures a number of addressable banks of a memory cell array.

39. (original) The method of claim 38 wherein the address circuitry routes an externally provided address signal to either a bank address decoder or a row address decoder.

40. (original) The method of claim 38 wherein the memory device comprises X rows, Y columns and Z banks, where the array comprises X*Y*Z memory cells.

41. (original) The method of claim 40 where the Z banks are configurable to 2, 4, 8 or 16 banks.

42. (original) A method of operating a memory system comprising:

outputting decode circuitry data from a processor to a memory device, wherein the decode circuitry decodes an external input signal to generate bank count data; and

adjusting address circuitry of the memory device in response to the decoded external input signal, wherein the address circuitry configures a number of addressable banks of a memory cell array using the bank count data.

43. (original) The method of claim 42 wherein the external input signal data comprises one bit of data.

44. (original) The method of claim 42 wherein the address circuitry routes externally address signals provided by the processor to either a bank address decoder or a row address decoder of the memory device.